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Page 1 of 3 ATTY. DOCKET NO. APPLICATION NO. SP018.C4 09/188,708 FORM PTO-1449 APPLICANT Garg et al. INFORMATION DISCLOSURE STATEMENT FILING DATE GROUP November 10, 1998 2783 U.S. PATENT DOCUMENTS EXAMINER CLASS SUB-CLASS FILING DATE INITIAL DOCUMENT NUMBER DATE NAME 07/1980 364 706 AA1 4,212,076 Conners AB1 5,125,092 06/1992 Prener 395 **725** 800 04/1993 Daniel et al. 395 AC1 5,201,056 AD1 5,241,636 08/1993 Kohn 395 375 395 375 AE1 5,487,156 01/1996 Popescu et al. 5,493,687 02/1996 Garg et al. 395 800.23 AF1 **39**5 5,560,035 09/1996 Garg et al. 800.23 AG1 AH1 5,682,546 Garg et al. 395 800.23 10/1997 ΑI ΑJ AK FOREIGN PATENT DOCUMENTS EXAMINER COUNTRY SUB-CLASS TRANSLATION DOCUMENT NUMBER CLASS INITIAL DATE 0 170 284 EΡ AL1 02/1986 0 213 843 03/1987 EP Yes AM1 No ΕP ANI 0 241 909 10/1987 Yes No OTHER (Including Author, Title, Date, Pertinent Pages, etc.) AR 1 Patterson et al., "A VLSI RISC," IEEE Computer, vol. 15, no. 9, pp. 8-18, September 1982. Maejima et al., "A 16-bit Microprocessor with Multi-Register Bank Architecture," Proc. Fall Joint AS 1 Computer Conference, Nov. 2-6, 1986, pp. 1014-1019. Birman et al., "Design of a High-Speed Arithmetic Datapath," IEEE, pp. 214-216, 1988. AT 1 Ruby B. Lee, "Precision Architecture," IEEE Computer, pp. 78-91, January_1989... AU 1 LARRY D. DONAGHUE EXAMINER DATE CONSIDERED PRIMARY EXAMINED Draw Line through EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609 citation if not in conformance and not considered. Include copy of this form with next communication to applicant.

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